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RESEARCH PAPER

Microstructural, chemical bonding, stress development and charge storage characteristics of Ge nanocrystals embedded in hafnium oxide

S. Das · R. K. Singha · S. Manna · S. Gangopadhyay · A. Dhar · S. K. Ray

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Abstract We have grown Ge nanocrystals (NCs) (4.0–9.0 nm in diameter) embedded in high-k HfO_2 matrix for applications in floating gate memory devices. X-ray photoelectron spectroscopy has been used to probe the local chemical bonding of Ge NCs. The analysis of Ge–Ge phonon vibration using Raman spectroscopy has shown the formation of compressively stressed Ge NCs in HfO_2 matrix. Frequency dependent electrical properties of HfO_2/Ge-NCs in HfO_2/HfO_2 sandwich structures have been studied. An anticlockwise hysteresis in the capacitance–voltage characteristics suggests electron injection and trapping in embedded Ge NCs. The role of interface states and deep traps in the devices has been thoroughly examined and has been shown to be negligible on the overall device performance.

Keywords X-ray photoelectron spectroscopy · Raman spectroscopy · Germanium nanocrystals · Charge injection

S. Das · R. K. Singha · S. Manna · A. Dhar · S. K. Ray (✉)
Department of Physics and Meteorology, Indian Institute of Technology Kharagpur, Kharagpur 721302, India
e-mail: physkr@phy.iitkgp.ernet.in

S. Gangopadhyay
School of Physics and Astronomy, University of Nottingham, University Park, Nottingham NG7 2RD, UK

Introduction

Nanocrystal floating gate devices are attractive due to their potential applications in next generation integrated flash memories. In these devices, metal or semiconductor nanocrystals (NCs) are embedded as charge-storage nodes in an oxide layer between the control gate and the tunneling layer to replace the continuous floating gate layers in conventional flash memories (Hanafi et al. 1996; Hori et al. 1992). The use of NCs as floating gates offers smaller operating voltages, better endurance characteristics and faster write/erase speeds as compared to conventional flash memories (Hanafi et al. 1996; Kim et al. 2003a; Blauwe 2002). Semiconductors as well as metals such as Si, Ge, SiGe, Ni, Au and Ag have been considered as promising candidates for the charge storage nodes in nanocrystal floating gate devices (Hanafi et al. 1996; Hori et al. 1992; Kim et al. 2003a; Blauwe 2002; Choi et al. 2002; Das et al. 2004; Park et al. 2006; Tan et al. 2005; Wang et al. 2007). Due to the smaller band-gap, superior carrier mobilities and higher excitonic Bohr radius compared to Si, Ge NCs are considered to be ideal nodes for use in complementary metal-oxide-semiconductor compatible memory circuits. They can be embedded in a high-k dielectric, which acts as the control oxide of a memory device with enhanced gate coupling to the tunneling oxide, resulting in an enhancement of memory window at a lower programming voltage (Compagnoni et al. 2003). Ge NCs embedded in Hf-based dielectrics, one of the most

attractive and promising high-k dielectrics, have been studied only recently (Chen et al. 2005; Zhang et al. 2006; Das et al. 2007b). Being physically much thicker than SiO_2, the leakage current of HfO_2 is several orders of magnitude smaller than SiO_2 for the same equivalent oxide thickness (EOT) (Lee et al. 2000), resulting in superior data retention behavior. On the other hand, HfO_2 can provide a larger tunneling current than SiO_2 during program operation, due to the lower electron barrier height of HfO_2 (1.2 eV) (Zhu et al. 2002) as compared to SiO_2 (3.1 eV).

Capacitance–voltage (C–V) measurement of memory capacitors has been an attractive method for obtaining device characteristics due to the ease of experimental setup and data analysis. However the conductance–voltage (*G–V*) characteristics of metal–oxide–semiconductor (MOS) capacitor is known to provide information directly related to the energy loss, in response to the applied ac signal, during the capture and emission of carriers by interface traps. Recently, a few groups (Huang et al. 2003; Ng et al. 2006) have reported energy loss by NCs during *G–V* measurements of memory capacitor. In this article, we present a detailed investigation of the charging, discharging and charge-retention behaviors in a trilayer HfO_2/Ge-NCs-embedded HfO_2/HfO_2 sandwiched memory capacitor using *C–V* and *G–V* measurements. The stress developed within the Ge NCs during solidification has been estimated by Raman spectroscopy.

Experiment

The memory structures used in this study was MOS capacitors with a dielectric stack consisting of Ge NCs sandwiched between tunneling and capping layers of HfO_2. P-type (100) Si substrate with resistivity 7–14 (cm was initially cleaned by Piranha process followed by dipping in dilute HF for 1 min to remove the native oxide from the surface. First, a thin tunneling layer of HfO_2 ($\sim$4 nm) was deposited on Si by rf magnetron sputtering technique from a 3 inch diameter HfO_2 (99.999% pure) target at 50 W rf power for 8 min in Ar + O_2 ambient. The intermediate layer was then deposited by co-sputtering of HfO_2 and Ge for 30 min under the same condition followed by the deposition of a final cap layer for 40 min. The trilayer structure was then subjected to thermal annealing in nitrogen ambient at 800 and 900 °C for 30 min.

High-resolution transmission electron microscopy (HRTEM) was carried out using a JEM 2100F (JEOL) field emission system with an operating voltage of 200 kV to study the micro-structural properties of Ge NCs in the trilayer structure. X-ray photoelectron spectroscopy (XPS) was used to probe the chemical bonding of the deposited films. XPS data was acquired using a SCIENTA ESCA 300 photoelectron (Al Kα radiation) spectrometer with an energy resolution of 0.4 eV using a pass energy of 150 eV and slit width 0.8 mm. Lower energy electrons (<3 eV) were supplied from a flood gun to prevent the charging. Raman spectra of the sample was obtained with a Renishaw Raman microscope equipped with a He–Ne laser excitation source emitting at a wavelength of 632.8 nm and a Peltier cooled (−70 °C) charge-coupled device (CCD) camera. The holographic grating (1,800 grooves/mm) and the slit provided a spectral resolution of 1 cm^{-1}. The electrical properties of the trilayer structure were carried out using fabricated Al-gate (area: 1.96×10^{-3} cm^2) MOS capacitor with programmable Keithley-590 *C–V* analyzer, Keithley-485 pico-ammeter and Advantest-R6144 constant dc voltage source. The *C–V* measurement of MOS capacitor at different frequencies was performed using a HP 4294A LCR meter.

Results and discussion

Microstructural studies

The microstructural property of Ge nanocrystal floating gate memory device was studied using cross-sectional HRTEM. Figure 1a shows a cross-sectional micrograph of sample annealed at 800 °C for 30 min in N_2 atmosphere. The dark patches are Ge NCs of 4–6 nm diameters in the HfO_2 matrix. The NCs are almost spherical and are well dispersed in the HfO_2 matrix. Figure 1a also suggests clustering of neighboring NCs in annealed sample. Figure 1b shows the TEM micrograph of a sample after annealed at 900 °C for 30 min. It shows Ge NCs with diameters 6–9 nm. Inset of Fig. 1b shows one such NC with clear lattice fringe. Note that there are few bigger clusters in Fig. 1b. Since the change in Gibbs free energy (ΔG) of the formation of GeO_2

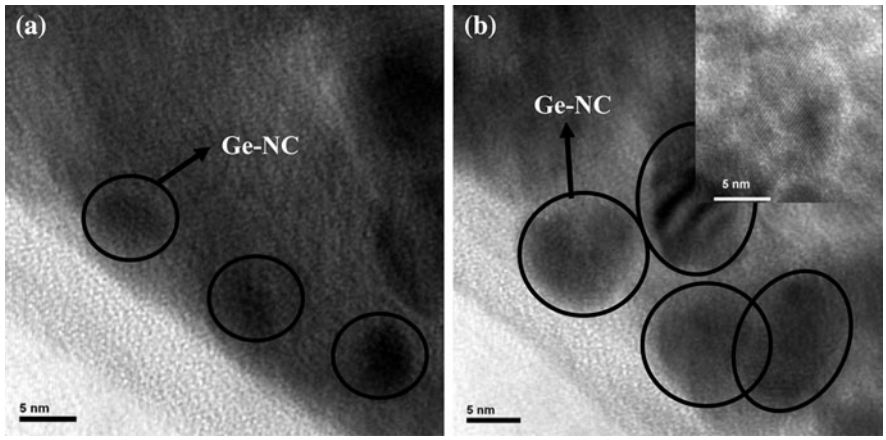

Fig. 1 Cross-sectional TEM micrograph of Ge NCs embedded in HfO_2 for **a** 800 °C and **b** 900 °C annealed sample

(−111.8 kcal/mol) is smaller than that of HfO_2 (−260.1 kcal/mol), ΔG is negative in solid reaction of $GeO_2 + Hf \rightarrow HfO_2 + Ge$. Hence, the mixture of HfO_2 and Ge has the lower Gibbs free energy in the co-sputtered film, resulting in the oxidation of Hf and agglomeration of Ge atoms into NCs in HfO_2 matrix.

The crystallization of all the films was investigated by X-ray diffraction (XRD) under grazing incidence. Figure 2 shows the XRD pattern of as deposited and annealed samples. The as-deposited sample has a broad scattering peak indicating its amorphous nature. Three peaks in both the annealed samples marked as (111), (220) and (311) in Fig. 2 correspond to the Bragg reflection of randomly oriented crystallites of Ge FCC structure. The broadening of the Bragg peak depends upon the crystallite size, strain and instrumentation broadening. The strain for the two annealed samples being different, it is very difficult to estimate the average crystallite size from only two data points, although instrumentation broadening can be deconvoluted. For annealed samples, germanium suboxides phases were present along with Ge cubic phase. We have not found any XRD peak related to HfO_2 phase.

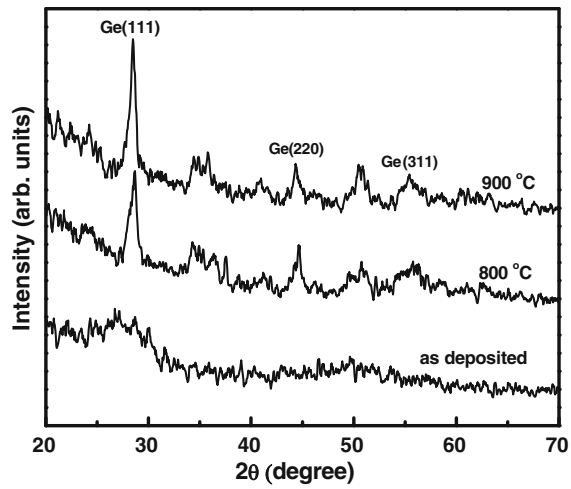

Fig. 2 X-ray diffraction pattern of as deposited and annealed samples

Chemical bonding of Ge nanocrystals

Figure 3 shows a typical Ge 3d X-ray photoelectron spectrum of the 900 °C annealed trilayer structure after 23 nm of sputter etching of the film. Five oxidation states, Ge^{n+} ($n = 0$–4) responsible for the Ge 3d XPS peak could exist in Ge-embedded oxides. Ge 3d XPS peaks from elemental Ge (Ge^0) and GeO_2 are usually observed at ~29 and ~32.2 eV, respectively. The shift of the Ge 3d peak (with respect to Ge^0) has been attributed to the formation of Ge–O, Ge–Hf–O and Ge–Hf bonds, as shown in the study of the Ge sub-oxides (Pourtois et al. 2008; Renault et al. 2007) and Ge/HfO_2 interface (Molle et al. 2006). The background of XPS spectrum in Figure 3 has been removed using a linear subtraction method and fitted by three Gaussian peaks at energy positions in agreement with the literature (Renault et al. 2007). The first one is assigned to the metallic Ge (Ge^0) around the binding energy 28.8 eV, and other two are oxide components of Ge. The peak shifted by 1.6 eV with respect to Ge^0 is related to Ge atoms in a 2+ oxidation state (GeO) and the other is assigned to Ge atoms in a GeO_2-like environment with 3.4 eV

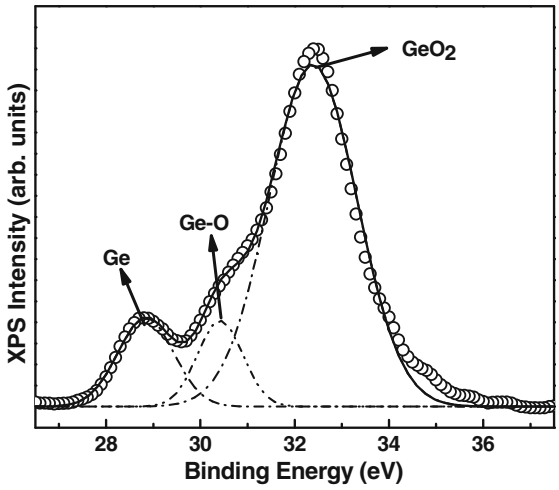

Fig. 3 Ge 3d XPS spectrum of 900 °C annealed sample after 23 nm of sputter etching

chemical shift. The chemical shifts found for both GeO and GeO_2 oxide states are consistent with an oxygen-induced core-level shift per Ge–O bond of 0.8 eV, in agreement with the previously reported value (Schmeisser et al. 1986). Ge^{+} and Ge^{3+} states are not observed most probably due to instability of the sub-oxide phases, favoring the formation of Ge^{4+} and Ge^{2+} states. A relatively high proportion of GeO_2 and GeO in our samples agree with those reported in SiO_2-embedded Ge (Das et al. 2007a). The result shows that germanium sub-oxides are formed at the interface between Ge NCs and HfO_2 matrix in co-sputtered intermediate layer.

Raman spectroscopy

Quantitative structural analysis can be achieved by Raman spectroscopy. Figure 4a shows the Raman spectra of HfO_2-embedded Ge NCs in the as-grown state and after post growth thermal annealing at 800 and 900 °C for 30 min in N_2 atmosphere. Raman spectra of NCs are characterized by size-dependent phonon confinement effects which, for the case of Si and Ge, are manifested by asymmetric line broadening and red shift of the peak due to breakdown of the $k = 0$ selection rule for Stokes scattering. The scattering peak at around 300 cm^{-1} is attributed to the crystalline Ge–Ge phonon vibration mode, indicating the formation of Ge NCs. The spectrum exhibits the expected asymmetric broadening in the lower wave number due to phonon confinement. However, the blue shift of the peak position with respect to that of the bulk reference spectrum is in disagreement with the prediction of phonon confinement theory. A similar blue shift of Raman spectra of silica-embedded (Sharp et al. 2005; Wellner et al. 2003) and sapphire-embedded (Sharp et al. 2006) Ge NCs has been reported, and is attributed to matrix-induced compressive stress on embedded NCs. The stress could arise due to the volumetric expansion of Ge during solidification (Wellner et al. 2003), fast growth rate experienced by NCs as a result of enhanced diffusivity (Choi et al. 2006) and from the interface energy. The hydrostatic pressure P in the NCs can be estimated as (Cerdeira et al. 1972)

$$P = \frac{(\omega_{\text{stressed}} - \omega_{\text{relaxed}})}{3\gamma\omega_0(S_{11} + 2S_{12})}, \tag{1}$$

where ω_{stressed}, ω_{relaxed} and ω_0 are the Raman shifts of stressed NCs embedded in HfO_2, relaxed NCs and pure bulk Ge, respectively; $\gamma = 0.89$ (Choi et al. 2006) is the mode-Grüneisen parameter, and S_{11} and S_{12} are components of the elastic compliance tensor with $S_{11} + 2S_{12} = 0.44 \times 10^{-12}$ $dyne^{-1}$ cm^2 (Choi et al. 2006). Since no suitable selective etchant for HfO_2 is available, the relaxed line position has been calculated using the phonon confinement model developed by Richter et al. (Richter et al. 1981). According to this model, the first order Raman spectrum of a NC can be described as a weighted contribution of phonon Lorentzians:

$$I(\omega) \propto \int \frac{|C(0,q)|^2}{[\omega - \omega(q)]^2 + \left(\frac{\Gamma_0}{2}\right)^2} \mathrm{d}q, \tag{2}$$

where q is the wave vector, $\omega(q)$ is the phonon dispersion curve, Γ_0 is the natural line width of the corresponding bulk material and $C(q)$ is the Fourier coefficient of the weighting function described as

$$|C(0,q)|^2 = \exp\left(\frac{q^2L^2}{16\pi^2}\right), \tag{3}$$

where L is the NC diameter. An expression for the average phonon dispersion of Ge within the Brillouin zone, $\omega(q)$, was calculated by Wellner et al. (2003), using the Brout sum method and neutron scattering data of Nilsson and Nelin, as (Wellner et al. 2003)

$$\omega(q) = \left(\omega_0^2 - \frac{43565 q_r^2}{|q_r| + 0.5766}\right)^{1/2}, \quad (4)$$

where $q_r = (a/2\pi)q$ is the reduced wave vector, a is the lattice parameter of bulk Ge, and ω_0 is the bulk zone center optical phonon frequency for isotopically enriched bulk ^{74}Ge. Figure 4b shows the experimental Raman spectrum of 900 °C annealed sample along with a simulated spectrum (solid line) calculated according to Eq. 2 with Fourier coefficients and phonon dispersion curve given by Eqs. 3 and 4, by taking 7 nm as the NCs average diameter. Calculated Raman peak for relaxed Ge (simulated curve) is found to be 296.3 cm^{-1} in comparison to the experimental value for embedded Ge of 304.6 cm^{-1} (circular symbol). The hydrostatic pressure P calculated using the above values from Eq. 1 is found to be about 2.4 GPa. From the Fig. 4a, it was also observed that the intensity of Ge–Ge phonon peak increases after post growth annealing. Although no stress relaxation is observed after either post growth annealing, which is generally observed for silica-embedded Ge NCs (Sharp et al. 2005). Same type of results also observed by Sharp et al. (2006) in sapphire-embedded Ge NCs. It is very important to understand stress development in high-k dielectric-embedded germanium nanocrystals as they have potential for memory device.

Charge injection and trapping in Ge nanocrystals

Ge nanocrystal trilayer capacitors have been utilized to capture the injected carriers from the channel, which cause a variation in the threshold voltage of the memory device. A relatively thicker blocking oxide is useful to prevent the carriers from gate electrode injecting into the charge trapping layer by Fowler–Nordheim tunneling. The schematic energy band diagram of the trilayer structure at flatband condition and under the +ve/−ve gate bias is shown in Fig. 5. The numerical values of band-gap and band offset are taken from the literature (Zhu et al. 2002; Chen et al. 2008). Under the +ve gate bias, electron current from the Si conduction band is enhanced using high-k HfO_2 as a blocking oxide. While in the −ve gate bias, the hole injection from the Si valance band can be enhanced and the electron current from the gate electrode can be suppressed using high-k HfO_2 as a blocking oxide. To get a high program/erase speed, the difference between electron and hole current should be higher. It is important to note that the back tunneling current can be suppressed using a large barrier height and high permittivity blocking oxide. Therefore, the high-k HfO_2 layer not only improves the charge trapping properties but also can improve the program/erase speed to facilitate device scaling.

Figure 6 shows the high frequency (100 kHz) C–V curves for 900 and 800 °C annealed sample for a sweep voltage of ±5.0 V. An anti-clockwise hysteresis characteristic is observed for both the sample indicating net electron trapping in the Ge NCs-embedded sandwich structure. A small flat-band voltage shift of 0.12 V is observed for the control sample without Ge NCs. However, a large memory window of 3.4 and 2.1 V are observed for 900 and 800 °C annealed sample, respectively, for a voltage sweep of ±5.0 V. Thus the effect of mobile ions on the charge trapping can be neglected. This suggests that the origin of C–V hysteresis can be attributed to injected charges mainly in NCs or at the interfaces between the NCs and the surrounding oxides, rather than the traps in HfO_2. A maximum flat band voltage

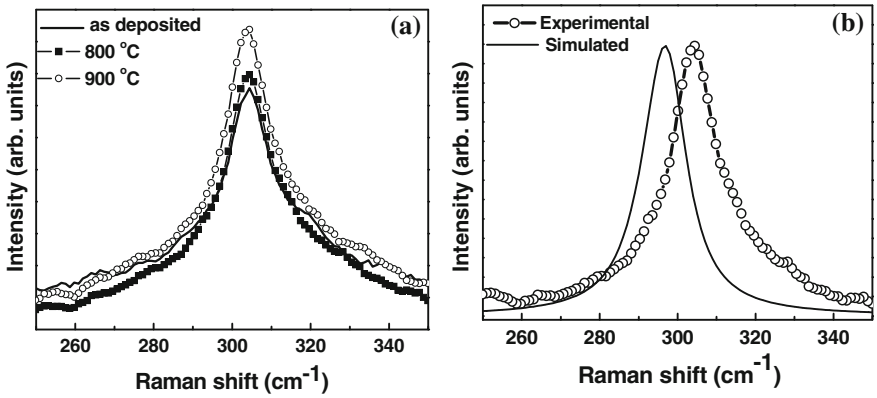

Fig. 4 **a** Raman spectra of the trilayer structure in the as-grown and annealed state. **b** Raman spectra of Ge NCs embedded in HfO_2 for 900 °C annealed sample (*open circle*), and *solid line* is the phonon confinement simulation for the case of fully relaxed NCs

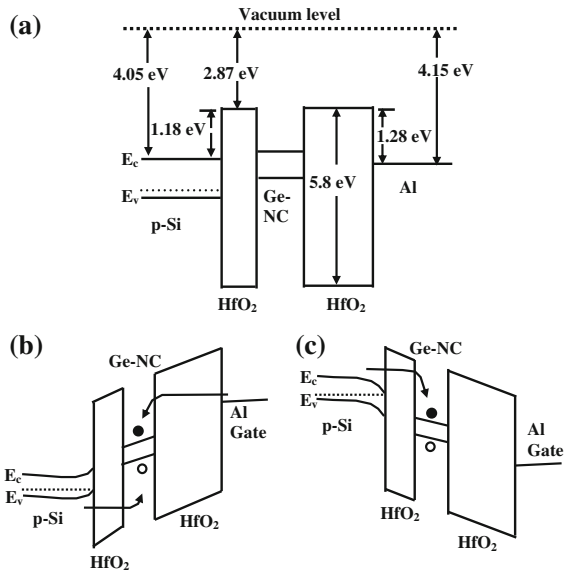

Fig. 5 Schematic energy band diagrams of p-Si/HfO_2/Ge-NC/HfO_2/Al memory structure at **a** flatband condition, and under **b** +ve and **c** −ve gate voltage

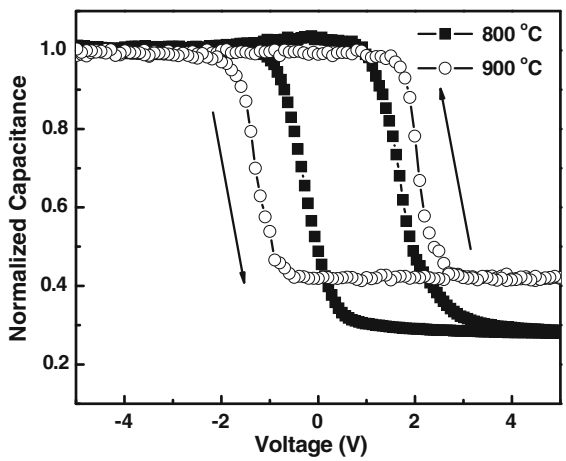

Fig. 6 High-frequency *C–V* characteristics of MOS capacitor with Ge nanocrystals in high-k HfO_2 matrix for 800 and 900 °C annealed sample

shift of 3.4 and 2.1 V obtained for NC-MOS devices give rise to a stored charge density N_{charge} of 7.9×10^{12} and 4.8×10^{12} cm^{-2}, respectively, using (Hori et al. 1992)

$$N_{charge} = \frac{\Delta V_{FB}}{\frac{q}{\varepsilon_0}\left(\frac{t_{CO}}{\varepsilon_{CO}} + \frac{t_{NC}}{\varepsilon_{NC}}\right)}, \quad (5)$$

where ΔV_{FB} is the flatband voltage shift, q is the magnitude of the electronic charge, t_{CO} and ε_{CO} are the thickness and relative permittivity of the control oxide, respectively, t_{NC} and ε_{NC} are the diameter and relative permittivity of the NC, respectively and ε_0 is the permittivity of the free space.

Although *C–V* measurement has been widely studied to obtain device characteristics due to the ease of experimental setup and data analysis, the *G–V* measurement is a relatively sensitive method and can provide further insights into the electrical operation of the devices (Sharp et al. 2005). Recently, Huang et al. (2003) and Ng et al. (2006) have reported energy loss by NCs during *G–V* measurements. Figure 7a and b shows the *C–V* and *G–V* characteristics of the trilayer MOS capacitor (900 °C annealed sample) for different sweep voltages. *G–V* curves show large conductance peak (G_p) shift and a large magnitude during the forward and reverse sweeping. This is explained by the larger gate capacitive coupling factor resulting from the higher dielectric constant HfO_2 cap layer. Since a higher electric field is channeled to the NCs from the applied gate bias, this results in more NCs being active in the conduction process (Ng et al. 2006). Conductance peak magnitude is also slightly larger for the reverse sweep as compared to that for the forward sweep. This could possibly be explained by the slightly larger electric field across the gate structure during the reverse sweep. From the *C–V* plot in Fig. 7a, the flatband voltage V_{FB} is determined for each sweep range and compared with the gate voltage value (V_{peak}), where the conductance peak occurs in the *G–V* plot in Fig. 7b. As observed in Fig. 8, V_{FB} tracks V_{peak} closely, that is the conductance peak occurs close to flatband voltage and in the depletion bias regime. This is because at depletion, the minority carrier density at the silicon tunnel dielectric interface is reduced. As a result, carrier capture rates slow down and Ge NCs cannot keep pace with the AC gate voltage, resulting in an energy loss. Hence, the energy loss is highest, when the conductance between the gate and silicon substrate peaks at a gate bias close to V_{FB}.

For a better understanding of the trapping characteristics, the frequency dependent *C–V* behavior has also been investigated for 900 °C annealed sample. Almost similar anti-clockwise *C–V* hysteresis in the frequency range 10 kHz to 10 MHz was observed in Fig. 9, which suggests that the hysteresis arises from the same origin. Moreover, there is no stretch-out in

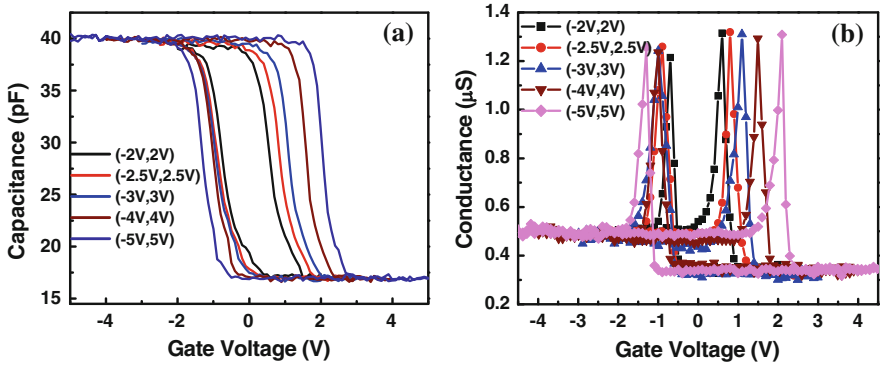

Fig. 7 High-frequency **a** *C–V* and **b** *G–V* characteristics of 900 °C annealed sample for different sweep voltages

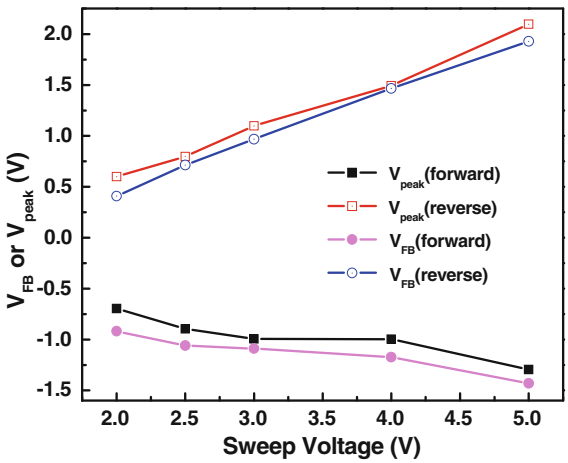

Fig. 8 Plot of the gate voltage corresponding to the conductance peak (V_{peak}) and flatband voltage (V_{FB}) from (*C–V* plot) versus the gate sweep voltage

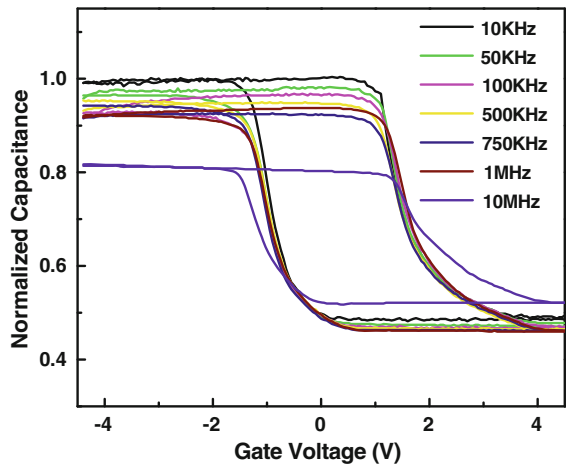

Fig. 9 Frequency dependent *C–V* characteristics at room temperature for 900 °C annealed sample

the *C–V* characteristics along the gate voltage axis for the entire experimental frequency range at room temperature. This is consistent with the fact that the hysteresis is not due to interface traps, as they generally give rise to frequency dependent *C–V* characteristics (Nicollian and Brews 1982). The observed frequency dispersion at higher frequencies in the accumulation region agrees well with the characteristics of HfO_2 based MOS capacitors. It is noted that these *C–V* curve have slightly different shape (e.g. slightly stretched) compared to those in Fig. 7a. This may be due to instrument variation, as we have performed frequency dependent *C–V* using a HP 4294A LCR meter and *C–V* for different sweep voltage by Keithley-590 *C–V* analyzer.

In order to investigate the discharging mechanism of charges in Ge NCs, capacitance versus time (*C–t*) measurement has been recorded and the result is presented in Fig. 10. Ge NCs-embedded MOS capacitor was initially charged for 5 s at a bias of −5 V, followed by *C–t* measurements by changing the gate voltage to the flat-band value. The discharging process is found to be logarithmic with time. The *C–t* curve consists of two regimes: the first is the initial fast decay, which may be due to the lateral charge loss (Winkler et al. 2002) and the Coulomb repulsion between electrons confined in NCs (Kim et al. 2003b). The slow decay in the second region is attributed to the leakage via tunneling barrier (Kim et al. 2003b). After 3.5×10^3 s, the capacitance decay is about 21 and 12% for 800 and 900 °C annealed sample, respectively. It has been seen that for higher temperature annealed sample, the initial fast decay is suppressed due to the complete isolation of Ge NCs (Kim et al. 2003b). To study the device stability, we have measured the endurance characteristics in Fig. 11 with ±5 V sweep voltage. We

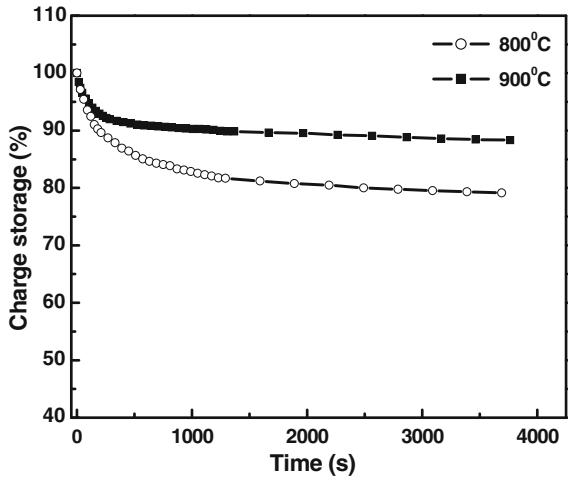

Fig. 10 Charge retention characteristics of the trilayer memory devices annealed at different temperature

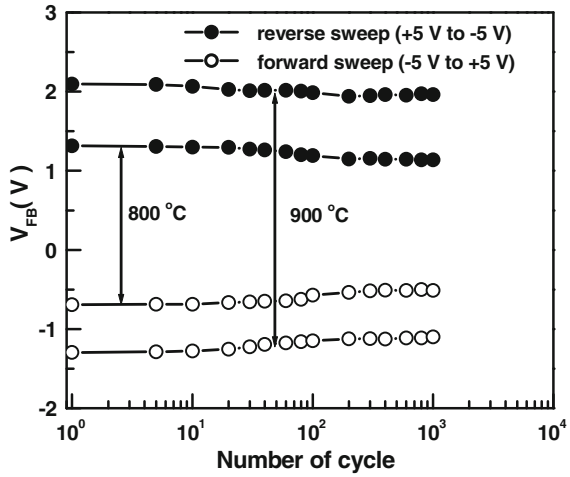

Fig. 11 Endurance characteristics of the memory devices for both 800 and 900 °C annealed samples

observed a slight decrease in the hysteresis after 10^3 cycles.

Conclusions

We have fabricated a trilayer HfO_2/Ge-NCs-embedded HfO_2/HfO_2 sandwiched memory structure using rf magnetron sputtering. The formation of spherically shaped NCs of 4.0–9.0 nm diameter has been observed using TEM microscopy. The probing of Ge 3d binding energy in XPS spectrum has indicated the presence of Ge NCs along with different oxidation states of Ge. The observed Ge phonon peak position in Raman spectra is influenced by the compressive stress and phonon confinement. The calculated stress of about 2.4 GPa originates from a liquid–solid phase transition of Ge during cooling. Sensitive electrical measurements of *C–V* and *G–V* have been utilized to investigate charging and discharging characteristics in Ge NCs. The observed shift in flatband voltage for *C–V* and conductance peak in *G–V* curves has been attributed to electron trapping in Ge NCs. Experimental data have shown that neither an interface defect nor a deep defect is dominant for the corresponding charging and discharging process. An improved memory retention time is observed in Ge NCs annealed under an optimum condition.

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References

Blauwe J (2002) Nanocrystal nonvolatile memory devices. IEEE Trans Nanotechnol 1:72–77

Cerdeira F, Buchenauer CJ, Pollack FH, Cardona M (1972) Stress induced shifts of first-order Raman frequencies of diamond- and zinc-blende-type semiconductors. Phys Rev B 5:580–593

Chen JH, Wang YQ, Yoo WJ, Yeo Y-C, Samudra G, Chan DSH, Du AY, Kwong D-L (2005) Nonvolatile flash memory device using Ge nanocrystals embedded in HfAlO high-k tunneling and control oxides: device fabrication and electrical performance. IEEE Trans Electron Devices 51:1840–1848

Chen HW, Chiu FC, Liu CH, Chen SY, Huang HS, Juan PC, Hwang HL (2008) Interface characterization and current conduction in HfO_2-gated MOS capacitors. Appl Surf Sci 254:6112–6115

Choi WK, Chim WK, Heng CL, Teo LW, Ho V, Ng V, Antoniadis DA, Fitzgerald EA (2002) Observation of memory effect in germanium nanocrystals embedded in an amorphous silicon oxide matrix of a metal-insulator-semiconductor structure. Appl Phys Lett 80:2014–2016

Choi WK, Chew HG, Zheng F, Chim WK, Foo YL, Fitzgerald EA (2006) Stress development of germanium nanocrystals in silicon oxide matrix. Appl Phys Lett 89:113126–113128

Compagnoni CM, Ielmini D, Spinelli AS, Lacaita AL, Gerardi C, Perniola L, Salvo B De, Lombardo S (2003) Program/erase dynamics and channel conduction in nanocrystal memories. IEDM Tech Dig 549–552

Das K, NandaGoswami M, Mahapatra R, Kar GS, Dhar A, Acharya HN, Maikap S, Lee J-H, Ray SK (2004) Charge storage and photoluminescence characteristics of silicon oxide embedded Ge nanocrystal trilayer structures. Appl Phys Lett 84:1386–1388

Das K, Goswami MLN, Dhar A, Mathur BK, Ray SK (2007a) Growth of Ge islands and nanocrystals using RF magnetron sputtering and their characterization. Nanotechnology 18:175301-1-5

Das S, Das K, Singha RK, Dhar A, Ray SK (2007b) Improved charge injection characteristics of Ge nanocrystals embedded in hafnium oxide for floating gate devices. Appl Phys Lett 91:233118–233120

Hanafi HI, Tiwari S, Khan I (1996) Fast and long retention-time nano-crystal memory. IEEE Trans Electron Devices 43:1553–1558

Hori T, Ohzone T, Odark Y, Hirase J (1992) A MOSFET with Si-implanted gate-SiO_2 insulator for nonvolatile memory applications. IEEE IEDM Tech Dig 92:469–472

Huang S, Banerjee S, Tung RT, Oda S (2003) Electron trapping, storing, and emission in nanocrystalline Si dots by capacitance-voltage and conductance-voltage measurements. J Appl Phys 93:576–581

Kim DW, Kim T, Banerjee SK (2003a) Memory characterization of SiGe quantum dot flash memories with HfO_2 and SiO_2 tunneling dielectrics. IEEE Trans Electron Devices 50:1823–1829

Kim JK, Cheong HJ, Kim Y, Yi JY, Park HJ (2003b) Rapid-thermal-annealing effect on lateral charge loss in metal-oxide-semiconductor capacitors with Ge nanocrystals. Appl Phys Lett 82:2527–2529

Lee SJ, Luan HF, Bai WP, Lee CH, Jeon TS, Senzaki Y, Roberts D, Kwong DL (2000) High-quality ultrathin CVD HfO_2 gate stack with poly-Si gate electrode. IEDM Tech Dig 31–34

Molle A, Bhulyan Md NK, Tallarida G, Fanclulli M (2006) In situ chemical and structural investigations of the oxidation of Ge(001) substrates by atomic oxygen. Appl Phys Lett 89:083504–083506

Ng TH, Chim WK, Choi WK (2006) Conductance-voltage measurements on germanium nanocrystals memory structures and effect of gate electric field coupling. Appl Phys Lett 88:113112–113114

Nicollian EH, Brews JR (1982) MOS physics and technology. Wiley, New York

Park CJ, Cho KH, Yang W-C, Cho HY, Choi S-H, Elliman RG, Han JH, Kim C (2006) Large capacitance-voltage hysteresis loops in SiO_2 films containing Ge nanocrystals produced by ion implantation and annealing. Appl Phys Lett 88:071916–071918

Pourtois G, Houssa M, Delable A, Conard T, Caymax M, Meuris M, Heyns MM (2008) Ge 3d core-level shifts at (100)Ge/Ge(Hf)O2 interfaces: a first-principles investigation. Appl Phys Lett 92:032105–032107

Renault O, Fourdrinier L, Martinez E, Clavelier L, Leroyer C, Barrett N, Crotti C (2007) High-resolution photoelectron spectroscopy of Ge-based HfO_2 gate stacks. Appl Phys Lett 90:052112–052114

Richter H, Wang ZP, Ley B (1981) The one phonon Raman spectrum in microcrystalline silicon. Solid State Commun 39:625–629

Schmeisser D, Schnell RD, Bogen A, Himpsel FJ, Roeger D, Landgren G, Morar J (1986) Surface oxidation states of germanium. Surf Sci 172:455–465

Sharp ID, Yi DO, Xu Q, Liao CY, Beeman JW, Liliental-Weber Z, Yu KM, Zakharov DN, Ager JW, Charzan DC, Haller EE (2005) Mechanism of stress relaxation in Ge nanocrystals embedded in SiO_2. Appl Phys Lett 86:063107-1-3

Sharp ID, Xu Q, Yi DO, Yuan CW, Beeman JW, Yu KM, Ager JW, Chrzan DC, Haller EE (2006) Structural properties of Ge nanocrystals embedded in sapphire. J Appl Phys 100: 114317-1-7

Tan Z, Samanta SK, Yoo WJ, Lee S (2005) Self-assembly of Ni nanocrystals on HfO_2 and N-assisted Ni confinement for nonvolatile memory application. Appl Phys Lett 86: 013107–013109

Wang C–C, Chiou Y–K, Chang C–H, Tseng J–Y, Wu L–J, Chen C–Y, Wu T–B (2007) Memory characteristics of Au nanocrystals embedded in metal-oxide-semiconductor structure by using atomic-layer-deposited Al_2O_3 as control oxide. J Phys D 40:1673–1678

Wellner A, Paillard V, Bonafos C, Coffin H, Claverie A, Schmidt B, Heinig KH (2003) Stress measurement of germanium nanocrystals embedded in silicon oxide. J Appl Phys 94:5639–5642

Winkler O, Merget F, Heuser M, Hadam B, Baus M, Spangenberg B, Kurz H (2002) Concept of floating-dot memory transistors on silicon-on-insulator substrate. Microelectron Eng 61:497–503

Zhu WJ, Ma T-P, Tamagawa T, Kim J, Di Y (2002) Current transport in metal/hafnium oxide/silicon structure. IEEE Electron Device Lett 23:97–99