Resonant tunneling diode circuits using Pspice

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Abstract

The measured \( I-V \) data and the large-signal equivalent circuit of a resonant tunneling diode are exploited, through the analog behavioral modeling capabilities of Pspice, to create a Pspice compatible model for the diode. The model is used, with very few other components, in the simulation of a number of circuit applications including a sinusoidal wave generator, a frequency multiplier and three state logic circuits. The simulated circuit details, the related waveforms and three-state logic operations are described. The circuits are characterized mainly by their reduced complexity and ease of analysis.

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1. Introduction

RTD physical models are mostly based on time dependent Schrödinger equation solved self-consistently with the Poisson equation. These models are usually not suitable for circuit design mainly due to the extremely long calculation times required. For circuit design, we usually know the electrical behavior of a given device but need some way to describe it in a simple but effective manner.

Although Pspice does not include a built-in model for a resonant tunneling diode, various ways can be used to implement and incorporate a suitable RTD model [1–3]. Three different ways have been used in the present work to obtain a Pspice-compatible model for the RTD. They are all based on the experimental \( I-V \) characteristics of the RTD and its large signal equivalent circuit. This model is then used to simulate a variety of circuits consisting mainly of a sinusoidal signal generator, a three state OR gate, a three state inverter and a frequency multiplier. The analyzed circuits are characterized mainly by their reduced complexity and ease of analysis.

2. Device \( I-V \) characteristics and Pspice models

The current–voltage data used in this simulation work are obtained from DBRT diodes grown by molecular beam epitaxy at Nottingham University. These are AlAs/GaAs/AlAs single well, double barrier structures grown on \( n+ \) Si-doped GaAs substrates. The mesa diameters of the structures were 20 \( \mu m \) and were mounted in a TO5 header packages.

The measured current versus voltage at room temperature is shown in Fig. 1. Shown also on the same figure are the fits to experimental data using both a polynomial function and a physically based equation (given below).

The basic large signal RTD equivalent circuit, widely published, consists mainly of an intrinsic part represented by a dynamic resistance in parallel with a capacitance plus a series conductance and series resistance to account for extrinsic effects. The capacitance accounts for both the charge accumulation in the quantum well and the depletion capacitance beyond the barrier regions [4]. An experimental method described in Ref. [5] was used to evaluate the equivalent circuit parameters and yield the values of the \( R_s \), \( C \) and \( L_s \) associated with the device structure. These were assumed voltage independent and were estimated to be 3.6 \( \Omega \), 1.5 pF and 0.75 nH, respectively. These relatively high values were mainly attributed [6] to packaging of the discrete device.

Using the built-in options GPOLY, GVALUE and GTABLE, part of the analog behavioral modeling capabili-
ties of Pspice [7], the $I-V$ characteristic is exploited to implement RTD models that can be used in designing a variety of reduced-complexity circuits. All the three options were implemented and used in the simulated circuits with no noticeable difference in their performance.

Although the polynomial representation of data has no physical justification, it has plenty of mathematical flexibility. This built-in capability allows controlled sources to be defined with a polynomial transfer function of any degree and any dimension. The GPOLY is used, in this context, to mimic the RTD with a high order polynomial. The coefficients of the polynomial were obtained by curve fitting the $I-V$ data. A 15th order polynomial was necessary to obtain a fairly acceptable fit.

The GVALUE option allows an instantaneous transfer function to be written as a mathematical expression in standard notation. It takes the input signal, performs the function specified by the mathematical expression on the signal, and outputs the result on the output pins.

An approximate equation to describe the large signal RTD behavior is based on the well-known Breit–Wigner formula of electron transmission through a double barrier structure. This Pspice-compatible equation is given in Ref. [8] as:

$$I = f \left\{ C_1 V \left[ \tan^{-1} (C_2 V + C_3) \right] - \tan^{-1} (C_2 V + C_4) \right\} + C_5 V^m + C_6 V^n$$

With $C_i$ are constants related to the peak and valley currents and voltages, $f$ is a scaling factor and $m$ and $n$ are integers. Fitting the above equation to the experimental $I-V$ data resulted in the following parameters: $m = 1$, $n = 5$, $f = 1$, $C_1 = 3.7 \times 10^{-3}$ A V$^{-1}$, $C_2 = 12.4$ V$^{-1}$, $C_3 = -3.9$, $C_4 = -12.8$, $C_5 = 1.5 \times 10^{-3}$ A V$^{-1}$, $C_6 = 3.9 \times 10^{-4}$ A V$^{-5}$.

The GTABLE part uses a transfer function described by a table consisting of pairs of the measured voltages and currents. The number of points taken by Pspice, although limited, was satisfactorily enough to include the important features of the $I-V$ curve.

In all cases the RTD is created as a sub-circuit consisting of a four terminal device in parallel with a capacitor and in series with $R_s$ and $L_s$. An appropriate symbol was then assigned to this new device and added to the Pspice library.

3. Application circuits

3.1. Sinusoidal signal generator and transient analysis

In the oscillator circuit proposed in Fig. 2(a), there should be, in principle, no input signal generator and in practice we rely on some initial transient or ultimately noise to start off the oscillations. There are no such sources in PSpice simulation, hence the necessity to introduce a Vpulse to provide the initial stimulus. The pulse period of this source is so large that only the first pulse counts.

![Fig. 2. (a) A resonant-tunneling diode-based oscillator circuit. (b) The output waveform of the RTD based oscillator.](image-url)
The output voltage at the 50 Ω termination is displayed in Fig. 2(b). As expected, the circuit approaches the quiescent bias point and oscillations begin to build and are setup after 1 μs the time delay specified in Vpulse. But once triggered the oscillations are observed to grow with time until they stabilize after 1.06 μs. The steady state oscillations are a perfect 600 mV peak-to-peak sinusoidal signal (inset of Fig. 2(b)). The period of the signal is under 1 ns, which corresponds to a frequency well over 1 GHz.

The frequency response in the present case is constrained mainly by the practical external-elements (Rs, Ls and Cs) associated with the packaging of the discrete diode and which were included in the diode’s PSpice model used in the simulation.

It is to be noted that varying the bias voltage, in particular, leads to output waveforms that are consistently sinusoidal but the amplitudes and periods of which are weakly bias dependent. Obviously, no oscillations were observed for voltages higher than the RTD valley voltage (Vc ≈ 1.17 V).

### 3.2. Three state circuits

The increasing need for reduced complexity circuits with higher storage density, higher speed stimulated the emergence of multivalued logic (MVL) in which the number of logic states is greater than two.

It is in this context that RTDs, with two or more NDR regions, witnessed recently a revived interest in their multivalued logic applications. Some of the advantages and merits of the NDR logic family over conventional logic families were particularly highlighted in Ref. [9].

Two Pspice compatible RTDs were combined in series to obtain an I–V characteristic with two well-defined NDR regions having equal peak and valley currents (Fig. 3). An appropriate load line was chosen to intersect the I–V curve in five different points three of which (A, B and C) are stable and can be used to define three logic states. These correspond to bias voltages V_A = 0.75 V, V_B = 1.63 V and V_C = 2.45 V with corresponding currents I_A = 10 mA, I_B = 8 mA and I_C = 6 mA. To shift the operation point from one state to another, the applied input pulse should provide a current step ΔI such that ΔI + I_A(B) > I_p/RL with RL being the load resistance.

The discrete RTD combination can be used as the fundamental element in the simulation of a variety of three state circuit applications. The circuits have the common advantage of being of reduced complexity and require very few components.

The first example of a signal processing application based on such a device is the frequency multiplier shown in the inset of Fig. 4. The circuit requires only a load resistor (RL) and an optional DC bias for an initial selection of the operating point. The DC bias, if used, will just introduce a voltage offset such that the portion of the I–V characteristics between 0 and V_offset is not reproduced in Fig. 3. I–V characteristics of two RTDs combined in series.

Fig. 4. Pspice simulated frequency multiplier circuit with input and output waveforms.

Fig. 5. Pspice simulated three-state inverter circuit with input (x) and output (z) obeying z = 2 − x.
the output signal. For a sawtooth waveform at the input of period 6 $\mu$s, the output is also a sawtooth waveform with a period three times that of the input signal (Fig. 4). The frequency multiplication can be readily explained based on the $I$–$V$ characteristics with the load line above [10].

The circuit in the inset of Fig. 5 is a three state inverter consisting of the RTD combination, a capacitor to decouple the DC source ($V_2$) from the input ($V_1$) and two resistors for appropriate biasing.

The output $x$ (Fig. 5) is obeying the three-state inverter logic expression: $x = n - 1 - y$, where $n$ is the number of states (three in the present case). The circuit operation can be explained knowing that the output voltage here is directly proportional to the RTDs current. With the input low, the operating point is initially at A (Fig. 3) corresponding to a current $I_A$ which results in a high output state $V_H = I_A R_2$.

The transition from the low to the mid-state in the input signal forces the device to switch to point B leading to a mid-state output $V_M = I_B R_2$. The mid-to-high input pulse forces the device into state $C$ with a low current $I_C$ and a corresponding low output voltage $V_L = I_C R_2$.

A two-input, three-state OR gate is shown in Fig. 6(a). The DC supply $V_{ss}$ and the resistors $R_1$ and $R_2$ are used to set the appropriate load line while each of the diodes $D_1$ and $D_2$ prevents the flow of current back to the inputs $V_1$ and $V_2$.

The input and output waveforms are shown in Fig. 6(b) and follow, as indicated, the logic function $x + y = \max(x, y)$ explicitly represented in the truth table.

In order to emphasize the reduced complexity of these circuits, it is to be mentioned, that a conventional frequency multiplier would have required a phase lock loop and a frequency divider while conventional CMOS and TTL inverters and OR gates would have required several transistors and resistors.

In summary, based on the measured $I$–$V$ characteristics, a model for a discrete RTD was created in the Pspice library and successfully used in the simulation of a number of application circuits. The circuits operate at room temperature and of a considerable reduced complexity. The intrinsic properties of the RTD structure predict a switching time of the order of ps, while the response times of the simulated circuits are in the low ns range. This was essentially attributed to the external lumped elements included in the RTD equivalent circuit.

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References


